James Han

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Experience

Tesla - Embedded Software Intern **Jan 2026 – *Current***
C, Linux
- Firmware platforms

Geltech Labs Inc. - Lead Firmware/Software Engineer **Oct 2024 – Dec 2025**
C / C++, C#, ARM Cortex-M4, Python, RS232/485/SPI/I2C/USART, Altium, Solidworks
- Working full time at seed-stage startup while also pursuing Master's degree.
- Lead Firmware and PCB development for the Carousel hydrogel testing product, pre-alpha to pilot production.
- Perform critical component selection, system design, de-risking strategies, system integration, verification & validation vesting, assembly process development, and create high level system documents, block diagrams, and specification sheets for manufacturing partners.
- Write Baremetal C for Distributed MCU system and C# for Engineering GUI, write extensive documentation.
- Developed core bare-metal infrastructure, including clocks, register-level drivers, real-time state machines, and communication control. Write peripheral drivers for heating, fluidics, mechanics, weighing, and display systems.

Hyundai Mobis OTA Embedded/Software Engineer Intern **Jul 2024 – Aug 2024**
Rust, C++, Java, Linux Kernel, Bash, Markdown, Doxygen, Android (AOSP)
- Research In-place, Block-based, A/B dynamic partitions, EXT4 filesystem, directory, multi-image, differential patch file generation and full/regular update testing and development
- Write/automate documentation using markdown and doxygen outlining use of proprietary CLTs
- System profiling and trace analysis for IVI USB Update pipeline with atrace; bottom-up userspace tracing for optimization within updating process.
- Improved USB update process time by 54% by optimizing the chunk size (1MB to 32MB) sent in extracting/copying update file loop to reduce context switching.

Projects

Research Intern - Jishen Zhao STABLE lab **Sept 2025 – *Current***
AMD Mlir-Aie, AMD Iron, Xilinx Vivado, PYNQ-Z2, Python, HLS in C/C++
- Investigating Heterogeneous SoC, CPU/GPU/NPU parallelism, Computer Architectures for AI
- Profile different transformer operators to find bottlenecks, characterize processor architecture types for AI workloads
- Investigating Cloud Native KV-Cache, KV-Cache blending, Methods for long context

Syscall Intercept **Sept 2025-Present**
Rust, Linux Kernel, gVisor, ptrace, strace
- Porting parts of gVisor over to Rust for user-space syscall interception
- Implementing seccomp filtering, SIGSYS handlers, routed syscall emulater through parent monitor
- Implement OS-specific structs that implement Syscall Context traits, define sysmsg-like communication pipe between parent monitor and child.

MIPS Processor Optimization **Jan 2025 – Mar 2025**
System Verilog, Verilator
- Implemented 5 optimizations to the classical Hennesey and Patterson 5-Stage Processor.
- Instruction cache next-line prefetching, data cache stride prefetching with stream buffers,TAGE branch predictor, fetch-stage branch target buffer, and two-way superscalar processing.
- Thorough analysis and optimization of CPI, bp accuracy, i/d cache miss.

Drone **Sept 2024 – Dec 2024**
C, ATMega128rfa, Autodesk Fusion
- Created a drone from scratch.
- PCB schematic, component sourcing, layout, tapeout, and population
- PID motor actuation algorithm
- Enclosure and Mechanical Design

Acquired 2022 **Plots - party** **Aug 2021 - Feb 2022**
Dart, Node.js, Firebase, GCP

Education

University of California - San Diego **Aug 2021- Expected Jun 2026**
BS/MS in Computer Science and Engineering